Claims

What is claimed is:

1. A processor comprising:

classification circuitry; and

memory circuitry coupled to the classification circuitry and being configurable to store at least a portion of at least a given one of a plurality of packets to be processed by the classification circuitry;

wherein the classification circuitry is configurable to implement a non-sequential packet classification process for at least a subset of the plurality of packets including the given packet.

2. The processor of claim 1 wherein the given packet is generated in accordance with multiple embedded protocols, and the non-sequential packet classification process allows the processor to return from a given point within the packet at which a final one of the protocols is identified to a beginning of the packet.

3. The processor of claim 2 wherein the given point within the packet comprises a point at which a Transmission Control Protocol (TCP) destination is identified.

4. The processor of claim 1 wherein the non-sequential packet classification process is implementable without loss of any portion of the packet.

5. The processor of claim 1 wherein the non-sequential packet classification process comprises execution of at least one skip to beginning instruction that allows the processor to skip back to a particular bit of the given packet at a time during the classification process after which the particular bit has been processed, such that multiple passes of the classification process can be performed on the given packet.

6. The processor of claim 5 wherein the skip to beginning instruction is executable in the processor under the control of an external host device operatively coupled to the processor.

7. The processor of claim 1 wherein the processor is configurable to provide an interface between a network from which the packets are received and a switch fabric.

8. The processor of claim 1 wherein the memory circuitry comprises an internal memory of the processor configurable to store a designated portion of the given packet and an external memory coupled to the processor and configurable to store substantially the entire given packet.

9. The processor of claim 1 wherein the classification circuitry comprises at least a first pass classifier and a second pass classifier, the non-sequential packet classification process being implementable in at least the second pass classifier.

10. The processor of claim 9 wherein the first pass classification comprises at least one of a reassembly operation, a parity check and a priority determination.

11. The processor of claim 9 wherein the first pass classification generates information which is passed in a specified data structure to the second pass classifier for use in the non-sequential packet classification process.

12. The processor of claim 1 wherein the processor comprises a network processor.

13. The processor of claim 1 wherein the processor is configured as an integrated circuit.

14. A method for use in a processor comprising classification circuitry and memory circuitry coupled to the classification circuitry, the method comprising the steps of:

storing in the memory circuitry at least a portion of at least a given one of a plurality of packets to be processed by the packet classification circuitry;

configuring the packet classification circuitry to implement a non-sequential packet classification process for at least a subset of the plurality of packets including the given packet.

15. The method of claim 14 wherein the given packet is generated in accordance with multiple embedded protocols, and the non-sequential packet classification process allows the processor to return from a given point within the packet at which a final one of the protocols is identified to a beginning of the packet.

16. The method of claim 14 wherein the non-sequential packet classification process is implementable without loss of any portion of the packet.

17. The method of claim 14 wherein the non-sequential packet classification process comprises execution of at least one skip to beginning instruction that allows the processor to skip back to a particular bit of the given packet at a time during the classification process after which the particular bit has been processed, such that multiple passes of the classification process can be performed on the given packet.

18. The method of claim 14 wherein the classification circuitry comprises at least a first pass classifier and a second pass classifier, the non-sequential packet classification process being implementable in at least the second pass classifier.